Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	49	("5752006" "5787007" "5933023" "5386156" "5430734" "5469003" "5500609" "5528176" "5552722" "5654650" "5670897" "5760719" "5786710" "5798656" "5811989" "5831448" "5844422" "5861761" "5869982" "5917337" "6075745" "6157557" "6191613" "6255849" "6278289" "6288568" "6292018" "6297665" "6323682" "6346825" "6351143" "6373279" "6388466" "6445209" "6897676" "6907595" "6101132" "6144220" "6147890" "5619728" "5623217" "5744980" "6215689" "6215689" "6282127" "6522167" "6662285" "6670826" "5870586" "5414377").pn.	USPAT	OR	ON	2005/09/12 15:33
L2	25086	field adj programmable adj gate adj array or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:33
L3	498953	bus or buss or busses	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:34
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L5	1124876	shift or shifted or shifting	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:34
L6	1262144	register or buffer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:35
L7	42116	state adj machine	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:35
L8	62449	instruction with L6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:35
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L21	2493	configuration adj logic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:53

L22	8	frame adj data adj input adj register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:54
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L33	5	19 and 20 and 21 and 22 and 23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 16:00
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Interconnection Networks Enable Fine-Grain Dynamic Multi-Tasking On FPGAs (2002) (Make Corrections) (9 citations)

Theodore Marescaux, Andrei Bartic, Diderick Verkest, Serge Vernalde, Rudy Lauwereins

Abstract: Multimedia support appears on embedded platforms, such as WAP for mobile phones. However, true multimedia applications require both the computation power that only dedicated hardware can provide and the flexibility of software implementations. To this end, we are investigating reconfigurable architectures, composed of an instruction-set processor running software processes and coupled to an FPGA on which hardware tasks are spawned by dynamic partial reconfiguration. This paper focuses on two... (Update)

Guaranteeing The Quality Of Services In Networks On Chip - Goossens, Dielissen, van .. (2003) (2 citations) (Correct)

.... **in decoupling and composing local solutions can be observed in hierarchical lay out and wiring, local clocking strategies such as GALS (globally asynchronous, locally synchronous) 6] software programmable fixed IPs or tiles [7, 8] and synthesisable tiles for dedicated silicon [9] or FPGAs [10, 11].** At the task level, these scalable system architectures (including e.g. chip multiprocessing [12, 13, 14] use tasks with local, independent address spaces and time frames that are composed by means of timingindependent fifo channels (for example, Kahn process networks for streambased ....

....switching to implement inter IP communication is expensive. **A** first optimisation is to use coarser circuits [47] to reduce the cost. **A packet switched interconnect with a predefined set of services allows sharing of communication resources, just like for ASICs, and enables dynamic reconfiguration [10, 11].** The NOC can be synthesised [10] but a preplaced hard wired NOC is the next logical step. **New** SOC architectures that rely on NOCs include chip multiprocessing [12, 13, 14, 7, 8, 48] to interconnect the homogeneous or heterogeneous tiles, and network processors [49] 6. **Conclusions** We observe ....

[Article contains additional citation context not shown here]

Th eodore Marescaux, Andrei Bartic, Dideriek Verkest, Serge Vernalde, and Rudy Lauwereins. *Interconnection networks enable fine-grain dynamic multitasking on FPGAs*. FPL, 2002. LNCS 2438.

Hierarchical Run-Time Reconfiguration Managed by an.. - Reconfigurable.. **Self-citation (Bartic Verkest Vernalde Lauwereins)** (Correct)

No context found.

T. Marescaux, A. Bartic, D. Verkest, S. Vernalde, R. Lauwereins, "*Interconnection Networks Enable FineGrain Dynamic Multi-Tasking on FPGA's*", FPL'02, p795-805, Montpellier, France.

Designing an Operating System for a Heterogeneous.. - Nollet Coene Verkest (2003) (7 citations) **Self-citation (Verkest Vernalde Lauwereins)** (Correct)

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Infrastructure for Design and Management of.. - Mignolet, Nollet.. (2003) (2 citations) **Self-citation (Verkest Vernalde Lauwereins)** (Correct)

....network plays an important role in our infrastructure, since it supports the communication of the system. **Networks on chip provide a solution for handling communication in complex systems on chip (SoC) We are studying packet switched interconnection networks for reconfigurable platforms [2].** To assist this research, we develop soft interconnection networks on commercial reconfigurable hardware. **They** are qualified soft because they are implemented using the reconfigurable fabric, while future platforms will use fixed networks implemented using standard ASIC technology. **This** soft ....

T. Marescaux, A. Bartic, D. Verkest, S. Vernalde and R. Lauwereins, "*Interconnection Networks Enable Fine-Grain Dynamic Multi-Tasking on FPGAs*", FPL'2002, pages 795805, Montpellier France.

Online Scheduling and Placement of Real-time Tasks to.. - Christoph Steiger.. (Correct)

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Heuristics for Online Scheduling Real-time Tasks to.. - Christoph Steiger.. (Correct)

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Rudy Lauwereins

Publisher Springer-Verlag London, UK

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Vincent Nollet , Théodore Marescaux , Diederik Verkest , Jean-Yves Mignolet , Serge Vernalde, Operating-system controlled network on chip, Proceedings of the 41st annual conference on Design automation, June 07-11, 2004, San Diego, CA, USA

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